Abstract

A variety of advantageous mechanisms for improved data transfer control within a data processing system are described. A DMA controller is described which is implemented as a multiprocessing transfer engine supporting multiple transfer controllers which may work

5   independently or in cooperation to carry out data transfers, with each transfer controller acting as an autonomous processor, fetching and dispatching DMA instructions to multiple execution units. In particular, mechanisms for initiating and controlling the sequence of data transfers are provided, as are processes for autonomously fetching DMA instructions which are decoded sequentially but executed in parallel. Dual transfer execution units within each transfer

10   controller, together with independent transfer counters, are employed to allow decoupling of source and destination address generation and to allow multiple transfer instructions in one transfer execution unit to operate in parallel with a single transfer instruction in the other transfer unit. Improved flow control of data between a source and destination is provided through the use of special semaphore operations, signals and message synchronization which may be invoked

15   explicitly using SIGNAL and WAIT type instructions or implicitly through the use of special "event-action" registers. Transfer controllers are also described which can cooperate to perform "DMA-to-DMA" transfers. Message-level synchronization can be used by transfer controllers to synchronize with each other.